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...capable to producing an activation of N-allylic substrates resulted in their double-bond [1,2]-migration and simultaneous **intra-substrate** hydrogen transfer[2]. While the catalytic properties of the mentioned complexes, in particular in alkene's oxidation...  
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...unit vector with direction from tip sphere centre K to substrate atom i. Functions  $VI(r_{ij})$  and  $VE(r_{iK})$  are the **intra-substrate** and interfacial atomic potentials, respectively. Numerical integration of equation (1) was accomplished via a leap-frog...  
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...middle substrate 38. An opening wall 52 surrounds opening 46 and extends between bottom and top surfaces 48 and 50. An **intra-substrate** conductor 54 resides on opening

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...the wafer scribe area, adjacent to the **active** portion of the chips.

&lsqb;0006&rsqb;...exclude the scribe area adjacent to the chip **active** area.

&lsqb;0007&rsqb; Still further...little information on components in the **active** area chip areas of the wafer. For example...

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(May 2004) Sagar Suresh Sabade, B.E., Pune University, India; M.Tech., Indian Institute of Science, Bangalore, India Chair of Advisory Committee: Dr.

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Oct 1996  
...manufacturing (Paper #: 2874-01) \* Inter- and **intra-die** polysilicon critical dimension variation...practice. !23 Paper #: 2874-02 Inter- and **intra-die** polysilicon critical dimension variation...the relative range and distribution of **intra-die**, or die-level, polysilicon critical dimension...  
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*Microelectronics Reliability*, Jan 1983  
...discussed in Part II. Thermosonic gold **wire bonding** to copper conductors. VERNON A...hybrid microcircuitry requires that **wire bonding** to their surfaces be demonstrated...of critical layers. Excellent **intra-die** overlay match is demonstrated...  
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**KNIGHT, Thomas, F. / SALZMAN, David, B. / KNIGHT, Thomas, F., PATENT COOPERATION TREATY APPLICATION**, Jan 1995  
...flip-chip, tape automatic bonding (TAB), or **wire-bonding**. In the MCM-C technologies,

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...layer enabling contacts of the Nb top **wiring** to the junction top electrode (central...characteristics (hysteresis: less than 7%), the **intra-wafer** parameter spread for j C is below...small contact holes and connecting a **wiring** layer within these holes without...

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2. [SINIS fabrication process for realizing integrated circuits in RSFQ impulse logic](#)  
**D Balashov / M I Khabipov / F-Im Buchholz / W Kessel / J Niemeyer**, *Superconductor Science and Technology*, Nov 1999  
...corresponding to  $LS = 0.94$  pH (**wiring-ground**),  $0.71$  pH (**wiring-base**) and  $0.58$  pH (base-ground) with **intrawafer** margins of  $LS = \pm 0...$  different types of **wiring** connection (see section...less than 10%) the **intrawafer** parameter spread is...

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...time extended past the nominal endpoint to compensate for: **intrawafer**-nonuniform etch rates nonuniform film thickness Typical over-etch...investigated for low- permittivity dielectrics for interconnect **wiring**.  
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